CLAIMS

What is Claimed is:

1. A system for testing the functionality of a plurality of integrated circuit dies formed in a plurality of rows on a semiconductor wafer, the system comprising:

a probe device having at least two probing areas configured to test the functionality of the plurality of dies, a first probing area of the at least two probing areas positioned to test each of a plurality of dies in a first row of the plurality of rows and a second probing area of the at least two probing areas positioned to test each of a plurality of dies in a second row of the plurality of rows simultaneously with the first probing area; and

a tester device coupled to the probe device and configured to compare test data received from the die in the first row with test data received from the die in the second row.

2. A system according to claim 1, wherein the comparison comprises an algorithm comparing functioning and nonfunctioning ones of the plurality of dies in the first row with a number of functioning and nonfunctioning ones of plurality of dies in the second row, and determining a percentage difference therefrom.

3. A system according to claim 2, wherein the testing device is further configured to signal a problem with a manufacturing process of the semiconductor wafer when the percentage difference exceeds a predetermined threshold value.

4. A system according to claim 2, further comprising a plurality of the first and second rows, wherein each of the first rows are adjacent to corresponding ones of the plurality of second rows.

5. A system according to claim 4, wherein the testing device comprises first and second computing portions corresponding to the first and second probing areas of the at least two probing areas.

6. A system according to claim 5, further comprising first and second control terminals coupled to the corresponding first and second computing portions.

7. A system according to claim 6, wherein the first and second control terminals are operable to input the algorithm.

8. A system according to claim 1, wherein each of the plurality of probing areas comprises at least one conductive contact configured to electrically contact at least one electrical contact pad associated with each of the plurality of dies.

9. A system according to claim 8, wherein the at least one conductive contact comprises at least one probe needle extending from each of the at least two probing areas.

10. A system according to claim 1, further comprising a database coupled to the testing device and configured to store the test data associated with the plurality of dies.

11. A system according to claim 1, wherein the probe device is a semiconductor wafer probe card.

12. A method of testing the functionality of a plurality of integrated circuit dies formed in a plurality of rows on a semiconductor wafer, the method comprising:

testing the functionality of each of a plurality of dies in a first row of the plurality of rows with a first probing area;

testing the functionality of each of a plurality of dies in a second row of the plurality of rows with a second probing area simultaneously with the testing of dies in the first row; and

comparing test data regarding the testing of dies in the first row with test data regarding testing of dies in the second row.

13. A method according to claim 12, wherein the comparing comprises comparing using an algorithm employable to compare a number of functioning and nonfunctioning ones of the plurality of dies in the first row with a number of functioning and nonfunctioning ones of plurality of dies in the second row, and determining a percentage difference therefrom.

14. A method according to claim 13, further comprising signaling a problem with a manufacturing process of the semiconductor wafer when the determining determines a percentage difference that exceeds a predetermined threshold value.

15. A method according to claim 13, further comprising testing the functionality of each of a plurality of dies in a plurality of first rows simultaneously with testing the functionality of corresponding ones of a plurality of dies in a plurality of second rows wherein each of the first rows are adjacent to corresponding ones of the plurality of second rows.

16. A method according to claim 15, further comprising comparing using first and second computing portions corresponding to the first and second probing areas.

17. A method according to claim 16, further comprising controlling the comparing using first and second control terminals coupled to the corresponding first and second computing portions.

18. A method according to claim 17, further comprising inputting the algorithm for the comparing using the first and second control terminals.

19. A method according to claim 12, further comprising testing the functionality of each of the plurality of dies in the first and second rows using at least one conductive contact

associated with each of the first and second probing areas and configured to electrically contact at least one electrical contact pad associated with each of the plurality of dies.

20. A method according to claim 19, wherein the at least one conductive contact comprises at least one probe needle extending from each of the at least two probing areas.

21. A method according to claim 12, further comprising storing the test data associated with the plurality of dies in a database.

22. A method according to claim 12, wherein the first and second probe areas are located on a semiconductor wafer probe card.